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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/803,043	03/18/2004	Ho-Cheol Lee	8947-000077/US	4619

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EXAMINER	
SANDVIK, BENJAMIN P	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 03/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/803,043	LEE, HO-CHEOL	
	Examiner	Art Unit	
	Ben P. Sandvik	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-18 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) 1-18 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1, 2, 5, 9, 10, 13,17, and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Imura et al (U.S. Patent #5949139), hereafter known as Imura.

With respect to **claim 1**, Imura teaches a semiconductor package in which multiple chips are embedded (Fig. 7), each chip including a common circuit having substantially the same common function (Fig. 1, 9 and 10; Col 5 Ln 24; Col 10 Ln 34), the common circuit in a selected one of the chips being enabled, the common circuit in one or more other chips being disabled, and the enabled common circuit performing the common function for the selected chips and the one or more other chips (Col 5 Ln 29-42).

With respect to **claim 2**, Imura teaches that at least one of the multiple chips is a semiconductor memory chip (Col 5 Ln 23).

With respect to **claim 5**, Imura teaches that multiple chips comprise two chips (Fig. 7).

With respect to **claim 6**, Imura teaches a common circuit that includes a power generator (Col 4 Ln 22).

With respect to **claim 8**, Imura teaches a common circuit that includes a signal generator (Col 4 Ln 22).

With respect to **claim 9**, Imura teaches Imura teaches a semiconductor package in which multiple chips are embedded (Fig. 7), each chip including a common circuit having substantially the same common function (Fig. 1, 9 and 10; Col 5 Ln 24; Col 10 Ln 34) and a selection circuit (Fig. 2), the common circuit in a selected one of the chips not being disabled via the corresponding selection circuit, the common circuit in one or more other chips being disabled via the corresponding selection circuit, and the non-disabled common circuit performing the common function for the selected chips and the one or more other chips (Col 5 Ln 29-42).

With respect to **claim 10**, Imura teaches that at least one of the multiple chips is a semiconductor memory chip (Col 5 Ln 23).

With respect to **claim 13,** Imura teaches that multiple chips comprise two chips (Fig. 7).

With respect to **claim 14**, Imura teaches a common circuit that includes a power generator (Col 4 Ln 22).

With respect to **claim 16**, Imura teaches a common circuit that includes a signal generator (Col 4 Ln 22).

With respect to **claim 17**, Imura teaches a method of reducing current consumption in a semiconductor package in which multiple chips are to be embedded, the method comprising: providing multiple chips, each chip including

a common circuit having substantially the same common function; enabling the common circuit in a selected one of the chips; disabling the common circuit in one or more other ones of the chips so as to reduce current otherwise consumed thereby; coupling the enabled common circuit and the one or more disabled common circuits such that the enabled common circuit performs the common function for the selected chip and the other chips (Col 2 Ln 27).

With respect to **claim 18**, Imura teaches that each of the chips includes a selection circuit (Col 5 Ln 55), the disabling of the common circuit in the one or more other chips includes coupling a disabling voltage to the selection circuit therein respectively, and the enabling of the common circuit in the selected chip includes not coupling a voltage to the selection circuit therein (Fig. 2, Col 5 Ln 62).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3, 4, 11, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Imura, in view of Butler (U.S. Patent #6392304).

With respect to **claim 3**, Imura teaches all of the limitations of claim 1, but does not teach that at least one of the multiple chips is a microprocessor chip.

Butler teaches a semiconductor package with multiple embedded chips where al least one of the chips is a microprocessor chip (Fig. 3, 10; and Col 4 Ln 34). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Imura and Butler to use a microprocessor chip in the semiconductor package of Imura in order to use the device to perform logic functions.

With respect to **claim 4**, Imura teaches all of the limitations of claim 1, but does not teach that at least one of the multiple chips is a microprocessor chip, and at least one of the other chips is memory chip. Butler teaches a semiconductor package wherein one of the chips is microprocessor chip (Fig. 3, 10; and Col 4 Ln 34), and one of the chips is a memory chip (Fig. 3, 18). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Imura and Butler to make the semiconductor package of Imura with at least one microprocessor chip and at least one memory chip in order to expand the functional capabilities of the semiconductor package.

With respect to **claim 11**, Imura teaches all of the limitations of claim 9, but does not teach that at least one of the multiple chips is a microprocessor chip. Butler teaches a semiconductor package with multiple embedded chips where al least one of the chips is a microprocessor chip (Fig. 3, 10; and Col 4 Ln 34). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Imura and Butler to use a

microprocessor chip in the semiconductor package of Imura in order to use the device to perform logic functions.

With respect to **claim 12**, Imura teaches all of the limitations of claim 9, but does not teach that at least one of the multiple chips is a microprocessor chip, and at least one of the other chips is memory chip. Butler teaches a semiconductor package wherein one of the chips is microprocessor chip (Fig. 3, 10; and Col 4 Ln 34), and one of the chips is a memory chip (Fig. 3, 18). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Imura and Butler to make the semiconductor package of Imura with at least one microprocessor chip and at least one memory chip in order to expand the functional capabilities of the semiconductor package.

Claims 7 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Imura, in view of Zhu (U.S. Patent #5866924).

With respect to **claim 7**, Imura teaches all of the limitations of claim 1, but does not teach a common circuit including a clock buffer. Zhu teaches a semiconductor package with multiple embedded chips (Fig. 9), wherein each integrated circuit has a clock buffer performing substantially the same function (Col 10 Ln 31). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Imura and Zhu in order to maintain clock synchronization in each individual chip.

With respect to **claim 15**, Imura teaches all of the limitations of claim 9, but does not teach a common circuit including a clock buffer. Zhu teaches a semiconductor package with multiple embedded chips (Fig. 9), wherein each integrated circuit has a clock buffer performing substantially the same function (Col 10 Ln 31). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Imura and Zhu in order to maintain clock synchronization in each individual chip.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ben P. Sandvik whose telephone number is (571) 272-8446. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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